ABSTRACT OF THE DISCLOSURE

A semiconductor device have memory cell array including a plurality of memory cells, each of which includes first and second transistors and connected in series between a bit line for normal access only and a bit line for refreshing only, and a capacitor connected to a connection node at which the first and second transistors are tied. A word line for normal access only and a word line for refreshing only are connected to control terminals of the first and second transistors, respectively. The semiconductor memory device has a late-write configuration in which writing to a memory cell at an externally input write address is performed, being delayed by a predetermined number of write cycles exceeding at least one, and has at least a circuit for checking whether the write address externally input the predetermined number of write cycles earlier matches the refresh address. If there is no hit as a check result, a write operation for activating the word line for normal access, turning on the first transistor, and writing data and a refresh operation for activating the word line for refreshing only, and refreshing using a sense amplifier for refreshing only, connected to the bit line for refreshing only are performed concurrently.